**Jiamin Gan (Jimmy)**

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**EDUCATION**

University of California, Berkeley BERKELEY, CA

***Master of Engineering, EECS – Physical devices and Integrated Circuits Anticipated May 2024***

University of Rochester ROCHESTER, NY

***Bachelor of Science, Electrical and Computer Engineering***

***Bachelor of Science, Computer Science May 2023***

* GPA: 3.96/4.00

**EXPERIENCE**

Expedera Inc. Santa Clara, CA

***Internship – RTL Design and Verification June 2022 – August 2022***

* Tested and debugged a switch fabric with AMBA buses, developed an automated script and an RTL checker
* Integrated a new IP for clock unit, interfaced using APB buses and control/status registers
* Verified floating-point unit using direct programming interface, developed C behavioral models
* Worked on a new AI accelerator architecture and synopsys-based ASIC design flow

University of Rochester ROCHESTER, NY

***Senior Design – Xillinx FPGA Implementation of AI Accelerator Januaray 2023 – May 2023***

* Implemented open sourced Nvidia Deep Learning Accelerator on KV260 using Xillinx Vivado design suit
* Coorperiate with teammate to develop cooresponding Petalinux operating system

University of Rochester ROCHESTER, NY

***Research Assistant – Exploring Possible SoC Architectures Januaray 2023 – May 2023***

* Assisted Quantum Inspired Computing circuit design
* Looked into ARM SoC architecture, Synopsys UVM library for AMBA buses verification

**SELECTED COURSEWORK**

**­­­­­Intro to VLSI Integcircuits:Degsn&Analysis Electronic Devices&Circuits**

**Multiprocessor Arch Mechatronics and Embedded Systems Login Design**

**Computer Organization Parallel & Distributed Systems Operating System**

**SELECTED PROJECT**

* ***Cadence VLSI simulation***

Used Cadence Virtuoso to simulate VLSI interconnect behaviors, analyzed the parasitic effects and power/clock distribution problems

* ***MIPS CPU using Verilog***

Used Verilog to construct a pipelined MIPS CPU that can execute MIPS instructions and executables compiled from C, simulated using Verilator

**SKILLS**

* Strong experience working with **System Verilog, C,** Python**,** Cadence Virtuoso
* Experienced in RTL development and waveform debugging using Synopsys tools
* Strong background in computer science and general programming, can easily pick up a new language in hours
* Familiar with Linux shell, good at writing shell scripts for higher productivity
* Good communication skills, repository organization with Git, strong report ability using LaTeX
* Language skills: Mandarin (native), English (fluent), Japanese (conversational)